Amendments To The Drawings

No amendments have been made to the drawings.

REMARKS

Claims 1-11, 15-16, 24-27, and 32-34 are pending. The Office Action dated January 9, 2006, in this Application has been carefully considered. The above amendments and the following remarks are presented in a sincere attempt to place this Application in condition for allowance. Claims 1-11, 15-16 and 24-27 have been amended, claims 32-34 have been added, and claims 12-14, 17-20, 22-23, and 28-31 have been cancelled in this Response. Applicant notes that the original application did not include a claim numbered '21.' Reconsideration and allowance are respectfully requested in light of the above amendments and following remarks.

Claims 10-12 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. In response thereto, Applicant notes that claim 12 is canceled herein, and claims 10-11 are amended herein. Applicant believes amended claims 10-11 are in condition for allowance.

Claims 1, 5-6, 8, and 15-16 were rejected under 35 U.S.C. 102(b) as being anticipated by Kalyanasundharam (US Patent Application Publication No. 2002/0133685). Applicant respectfully traverses this rejection. Claims 1 and 15 are independent claims. Pending claims 2-8 depend from claim 1, and pending claim 16 depends from claim 15.

Kalyanasundharam does not teach or disclose a method of storing an effective address (EA) in an effective to real address translation (ERAT) table, or an apparatus for translating an effective address to a real address, wherein the method involves adding a plurality of page size indicator (PSI) fields to each entry of the ERAT table, and wherein the PSI fields of each entry are used to store values that ***collectively specify either: (i) a page size of the EA, wherein the page size of the EA is one of the supported page sizes, or (ii) that the EA does not need translation***, and wherein ***at***

least one combination of the values of the PSI fields of each entry specifies that the effective address stored in the same entry does not need translation.

As amended herein, claim 1 recites (emphasis added):

1. A method of storing an effective address (EA) in an effective to real address translation (ERAT) table supporting multiple page sizes including a base page size, wherein the ERAT table comprises a plurality of entries, the method comprising the steps of:

adding a plurality of page size indicator (PSI) fields to each entry of the ERAT table, wherein the PSI fields of each entry are used to store values that ***collectively specify either: (i) one of the supported page sizes, or (ii) that an effective address stored in the same entry of the ERAT table does not need translation***, and wherein ***at least one combination of the values of the PSI fields of each entry specifies that the effective address stored in the same entry does not need translation***;

storing the EA in one of the entries of the ERAT table; and

setting the values of the PSI fields of the one of the entries of the ERAT table to specify either: (i) a page size of the EA, wherein the page size of the EA is one of the supported page sizes, or (ii) that the EA does not need translation.

As amended herein, claim 15 recites (emphasis added):

15. An apparatus for translating an effective address to a real address, comprising:

means for storing an effective to real address translation (ERAT) table having a plurality of entries each configured to store an effective address, a real address corresponding to the stored effective address, and a plurality of page size indicator (PSI) values that ***collectively specify either: (i) a page size of an effective address stored in the same entry of the ERAT table, wherein the page size of the effective address is one of a plurality of supported page sizes,***

or (ii) that an effective address stored in the same entry of the ERAT table does not need translation, wherein at least one combination of the PSI values of each entry specifies that the effective address stored in the same entry does not need translation;

means for receiving the effective address to be translated;

means for determining whether the received effective address requires translation; and

means for, in the event the received effective address does not require translation, outputting the received effective address as the real address;

means for, in the event the effective address requires translation, comparing each of a plurality of ranges of the received effective address to a corresponding range of an effective address stored in each entry of the ERAT table dependent upon the PSI values, wherein the received effective address is divided into the plurality of ranges dependent upon a number of the supported page sizes;

means for, in the event the effective address requires translation and each range of the received effective address matches a corresponding range of an effective address stored in a particular entry of the ERAT table dependent upon the PSI values:

selecting ranges of the real address stored in the particular entry of the ERAT table dependent upon the PSI values; and

outputting the real address, wherein the real address includes the selected ranges of the real address stored in the particular entry of the ERAT table.

Figure 1 of Kalyanasundharam shows a diagram of a conventional variable page size TLB 100 in combination with requisite peripheral circuitry. A representative page table entry 106 in a RAM 104 stores a validity bit ("V") 108, size-field bits ("SZ[1:0]") 110, physical address bits ("PA[40:13]") 112 and status bits ("STATUS[8:0]") 114. Figure 1A of Kalyanasundharam is a

table showing typical encoded size-field data for four different page sizes supported by the TLB 100 of Figure 1. As shown in Figure 1A, the size-field data consists of 2 bits, SZ[1:0], each different combination of these two bits representing a different page size.

Figure 1 of the instant application shows an ERAT table having an entry including a compare array entry 120 and a corresponding data array entry 138. The compare array entry 120 includes page size indicators (fields) R1 (122), R2 (124), and R3 (126). Table 1 shows how the PSI fields R1 (122), R2 (124), and R3 (126) store values that ***collectively specify either: (i) a page size of the effective address stored in the same entry, wherein the page size of the effective address is one of multiple supported page sizes, or (ii) that the effective address does not need translation.*** Table 1 also shows that ***a selected combination of the values of the PSI fields of each entry specifies that the effective address stored in the same entry does not need translation.***

Applicant asserts Kalyanasundharam does not teach or disclose an ERAT with entry fields used to store values that ***collectively specify either: (i) a page size of an effective address stored in the same entry, wherein the page size of the effective address is one of multiple supported page sizes, or (ii) that the effective address stored in the same entry does not need translation***, and wherein ***at least one combination of the values of the PSI fields of each entry specifies that the effective address stored in the same entry does not need translation.***

Regarding claim 2, Applicant asserts Kalyanasundharam does not disclose the method of claim 1, wherein a PSI field is added for each unique page size, including a base page size.

Regarding claim 4, Applicant asserts Kalyanasundharam does not describe the method of claim 1, wherein each entry of the ERAT table is also configured to store a plurality of state bits, and wherein all effective addresses that do not require translation and have the same state bits share the same entry of the ERAT table.

Regarding claim 6, Applicant asserts Kalyanasundharam does not disclose the method of claim 1, wherein (m+1) PSI fields are added to each entry of the ERAT table, and wherein m is an integer, and wherein m of the (m+1) PSI fields are used to store values that collectively specify one of the supported page sizes, and wherein the remaining one of the (m+1) PSI fields is used to store a value that specifies whether the an effective address stored in the same entry needs translation.

Regarding claim 7, Applicant asserts Kalyanasundharam does not describe the method of claim 6, wherein each of the (m+1) page size indicator (PSI) fields added to each entry of the ERAT table is configured to store one binary digit.

For at least the above reasons, Applicant asserts Kalyanasundharam fails to teach or disclose all of the elements and limitations of pending independent claims 1 and 15. Applicant also believes that pending claims 2-8 that depend from claim 1, and pending claim 16 that depends from claim 15, are also allowable for at least the above reasons.

Claims 10 and 18 were rejected under 35 U.S.C. 103(a) as being unpatentable over Kalyanasundharam and Kongetira (US Patent No. 6,078,987). Applicant respectfully traverses this rejection. Applicant notes claim 18 is canceled herein, and pending claims 10-11 depend from claim 9.

The combination of Kalyanasundharam and Kongetira does not teach or disclose a method for translating an effective address to a real address involving an ERAT table, wherein the ERAT table supports multiple page sizes including a base page size, and wherein the ERAT table has multiple entries each configured to store an effective address, a real address corresponding to the stored effective address, and a plurality of page size indicator (PSI) values that ***collectively specify either: (i) a page size of an effective address stored in the same entry of the ERAT table, wherein the page size of the effective address is one of a plurality of supported page sizes including a base***

page size, or (ii) that an effective address stored in the same entry of the ERAT table does not need translation, wherein at least one combination of the PSI values of each entry specifies that the effective address stored in the same entry does not need translation.

As amended herein, claim 9 recites (emphasis added):

9. A method for translating an effective address to a real address, comprising:

providing an effective to real address translation (ERAT) table having a plurality of entries each configured to store an effective address, a real address corresponding to the stored effective address, and a plurality of page size indicator (PSI) values that ***collectively specify either: (i) a page size of an effective address stored in the same entry of the ERAT table, wherein the page size of the effective address is one of a plurality of supported page sizes including a base page size, or (ii) that an effective address stored in the same entry of the ERAT table does not need translation, wherein at least one combination of the PSI values of each entry specifies that the effective address stored in the same entry does not need translation***;

receiving the effective address to be translated;

determining whether the received effective address requires translation; and

in the event the received effective address does not require translation, outputting the received effective address as the real address.

Kalyanasundharam is described above.

Kongetira describes a translation look aside buffer having separate RAM arrays which are accessible with separate enable signals.

Applicant asserts the combination of Kalyanasundharam and Kongetira does not teach or disclose an ERAT with entry fields used to store values that ***collectively specify either: (i) a page size of an effective address stored in the same entry, wherein the page size of the effective address***

is one of multiple supported page sizes, or (ii) that the effective address stored in the same entry does not need translation, wherein at least one combination of the PSI values of each entry specifies that the effective address stored in the same entry does not need translation.

For at least the above reasons, Applicant asserts the combination of Kalyanasundharam and Kongetira fails to teach or disclose all of the elements and limitations of pending independent claim 9. Applicant also believes that pending claims 10-11 that depend from claim 9 are also allowable for at least the above reasons.

Claims 13-14 and 22-23 were rejected under 35 U.S.C. 103(a) as being unpatentable over Kalyanasundharam and Mathews (US Patent No. 6,625,715). In response thereto, Applicant notes claims 13-14 and 22-23 are canceled herein.

Claims 24-25 were rejected under 35 U.S.C. 103(a) as being unpatentable over Kalyanasundharam and Lomax, Jr., et al. (US Patent Application Publication 2003/0204702). Applicant respectfully traverses this rejection. Applicant notes claim 24 is an independent claim, and claim 25 depends from claim 24.

The combination of Kalyanasundharam and Lomax, Jr., et al. does not teach or disclose a computer program product for storing an effective address (EA) in an effective to real address translation (ERAT) table, wherein the ERAT table supports multiple page sizes including a base page size, and wherein the product includes computer program code for adding a plurality of page size indicator (PSI) fields to each entry of the ERAT table, and wherein the PSI fields of each entry are used to store values that ***collectively specify either: (i) a page size of the EA, wherein the page size of the EA is one of the supported page sizes, or (ii) that the EA does not need translation***, and wherein ***at least one combination of the values of the PSI fields of each entry specifies that the effective address stored in the same entry does not need translation.***

As amended herein, claim 24 recites (emphasis added):

24. A computer program product for storing an effective address (EA) in an effective to real address translation (ERAT) table supporting multiple page sizes including a base page size, wherein the ERAT table comprises a plurality of entries, the computer program product having a medium with a computer program embodied thereon, the computer program comprising:

computer program code for adding a plurality of page size indicator (PSI) fields to each entry of the ERAT table, wherein the PSI fields of each entry are used to store values that ***collectively specify either: (i) one of the supported page sizes, or (ii) that an effective address stored in the same entry of the ERAT table does not need translation***, and wherein ***at least one combination of the values of the PSI fields of each entry specifies that the effective address stored in the same entry does not need translation***;

computer program code for storing the EA in one of the entries of the ERAT table; and

computer program code for ***setting the PSI fields of the one of the entries of the ERAT table to specify either: (i) a page size of the EA, wherein the page size of the EA is one of the supported page sizes, or (ii) that the EA does not need translation***.

Kalyanasundharam is described above.

Lomax, Jr., et al. discloses a method of operating a processing device, including defining an effective memory address space with a cached address space and a non-cached address space, wherein the cached address space and the non-cached address space each translate to overlap a single physical memory space. A memory address of the physical memory space is accesses without accessing a cache memory system from the non-cached effective address space. A memory address of the physical memory space is accessed from the cached effective address space with the benefit of the cache memory system. (Lomax, Jr., et al., Abstract.)

Applicant asserts neither Kalyanasundharam nor Lomax, Jr., et al. discloses an ERAT with entry fields used to store values that ***collectively specify either: (i) a page size of an effective address stored in the same entry, wherein the page size of the effective address is one of multiple supported page sizes, or (ii) that the effective address stored in the same entry does not need translation***, and wherein ***at least one combination of the values of the PSI fields of each entry specifies that the effective address stored in the same entry does not need translation.***

For at least the above reasons, Applicant asserts the combination of Kalyanasundharam and Lomax, Jr., et al. fails to teach or disclose all of the elements and limitations of pending independent claim 24. Applicant also believes that pending claim 25 that depends from claim 24 is also allowable for at least the above reasons.

Claim 27 was rejected under 35 U.S.C. 103(a) as being unpatentable over Kalyanasundharam and Lomax, Jr., et al. as applied to claim 24 above, and further in view of Kongetira. Applicant respectfully traverses this rejection. Applicant notes pending claim 27 depends from claim 26.

The combination of Kalyanasundharam and Lomax, Jr., et al. and Kongetira does not teach or disclose a computer program product for translating a received effective address to a real address, wherein the product includes computer program code for accessing an effective to real address translation (ERAT) table, and wherein the ERAT table has a plurality of entries each configured to store an effective address, a real address corresponding to the stored effective address, and a plurality of page size indicator (PSI) values that ***collectively specify either: (i) a page size of an effective address stored in the same entry of the ERAT table, wherein the page size of the effective address is one of a plurality of supported page sizes including a base page size, or (ii) that an effective address stored in the same entry of the ERAT table does not need translation***, and

wherein ***at least one combination of the PSI values of each entry specifies that the effective address stored in the same entry does not need translation.***

As amended herein, claim 26 recites (emphasis added):

26. A computer program product for translating a received effective address to a real address, comprising:

computer program code for accessing an effective to real address translation (ERAT) table to determine whether the received effective address requires translation, wherein the ERAT table has a plurality of entries each configured to store an effective address, a real address corresponding to the stored effective address, and a plurality of page size indicator (PSI) values that ***collectively specify either: (i) a page size of an effective address stored in the same entry of the ERAT table, wherein the page size of the effective address is one of a plurality of supported page sizes including a base page size, or (ii) that an effective address stored in the same entry of the ERAT table does not need translation***, and wherein ***at least one combination of the PSI values of each entry specifies that the effective address stored in the same entry does not need translation***;

computer program code for determining whether the received effective address requires translation; and

computer program code for, in the event the received effective address does not require translation, outputting the received effective address as the real address.

Kalyanasundharam, Lomax, Jr., et al., and Kongetira are described above.

Applicant asserts neither Kalyanasundharam nor Lomax, Jr., et al. nor Kongetira discloses an ERAT with entry fields used to store values that ***collectively specify either: (i) a page size of an effective address stored in the same entry, wherein the page size of the effective address is one of multiple supported page sizes, or (ii) that the effective address stored in the same entry does not***

need translation, and wherein ***at least one combination of the PSI values of each entry specifies that the effective address stored in the same entry does not need translation.***

For at least the above reasons, Applicant asserts the combination of Kalyanasundharam and Lomax, Jr., et al. and Kongetira fails to teach or disclose all of the elements and limitations of pending independent claim 26. Applicant believes that pending claim 27 that depends from claim 26 is also allowable for at least the above reasons.

Claims 30-31 were rejected under 35 U.S.C. 103(a) as being unpatentable over Kalyanasundharam and Lomax, Jr., et al. as applied to claim 24 above, and further in view of Mathews. In response thereto, Applicant notes claims 30-31 are canceled herein.

In the Office Action, the Examiner objected to claims 2-4, 7, 9, 17, 19-20, 26, and 28-29 as being dependent upon a rejected base claim, but noted claims 2-4, 7, 9, 17, 19-20, 26, and 28-29 would be allowable if rewritten in independent form.

With respect to claims to 2-4, the Examiner noted that Kalyanasundharam "...fails to teach of wherein a PSI field is added for each unique page size, including the base page size."

With respect to claim 7, the Examiner noted that Kalyanasundharam "...does not teach of a translation-disabled address not being stored in the ERAT."

With respect to claims 9, 17, and 26, the Examiner noted "The prior art does not teach of upon determining the EA is not translation-disabled, determining which EA ranges should match, in order for the EA to match the ERAT entry, by checking the PSI fields for each ERAT entry as stated in each claim."

With respect to claims 11, 19, and 28, the Examiner noted that Kalyanasundharam "does not teach of determining the page size of the EA after determining that the EA is not translation-disabled."

With respect to claims 12, 20, and 29, the Examiner noted Kalyanasundharam "...teaches of determining whether the EA matches and existing entry, and upon determining such, that entry is used and a new entry is not written, but Kalyanasundharam does not teach of doing it after determining that the EA is translation-disabled."

In the present response, Applicant addresses all of the claim objections and rejections cited in the Office Action. In view of the amendments to the claims and Applicant's remarks, Applicant believes pending claims 1-11, 15-16, 24-27, and 32-34 are in condition for allowance, and respectfully request allowance of pending claims 1-11, 15-16, 24-27, and 32-34.

With the amendments to the claims presented herein, there are currently 6 pending independent claims and 20 total pending claims in the application. As the original application had 3 independent claims and 30 total claims, Applicant believes additional fees are due.

Applicant has included a check in the amount of six hundred dollars ($600.00) to cover three (3) independent claims in excess of three. In the event that any other fees are due, the Commissioner is hereby authorized to charge any required fees due (other than issue fees), and to credit any overpayment made, in connection with the filing of this paper to Deposit Account No. 50-0605 of CARR LLP.

The present amendment is believed to contain a complete response to the issues raised in the Office Action. Full reconsideration is respectfully requested. If the Examiner should have any questions, comments or suggestions, the undersigned attorney earnestly requests a telephone conference. In particular, should the Examiner deem that any further amendment is desirable to place this application in condition for allowance, the Examiner is also invited to telephone the undersigned at the number listed below.

Respectfully submitted,

CARR LLP

Dated: 4/4/06

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